```
    .include <m2560def.inc>
    .equ    hiCnt = 1136    ; delay count for creating 880-Hz tone
    .equ    loCnt = 2273    ; delay count for creating 440-Hz tone
    .def    dlyHi = R20
    .def    dlyLo = R21
    .def    tmpH = R22
    .def    tmpL = R23
    .cseg
    .org    0x00
    jmp start
    .org    0x22
    jmp oc1AISR
    .org    0xF6
start:  ldi tmpH,low(RAMEND)    ; initialize the SP
    out SPL,tmpH        ;   "
    ldi r16,high(RAMEND)    ;   "
    out SPH,tmpH        ;   "
    ldi tmpH,0x20   ; configure OC1A/PB5 pin for output
    sts DDRB,tmpH   ;   "
    ldi tmpH,0x40   ; configure TMR1 to operate in normal mode with compare
    sts TCCR1A,tmpH ; match action set to toggle
    ldi tmpH,0x02   ; select clk_IO / 8 as clock input to Timer 1
    sts TCCR1B,tmpH ;   "
    ldi dlyHi,high(hiCnt)   ; initialize the delay count for the compare operation
    ldi dlyLo,low(hiCnt)    ; (use the delay count for 880-Hz)
    lds tmpL,TCNT1L ; read the 16-bit timer 1
    lds tmpH,TCNT1H ;   "
    add tmpL,dlyLo
    adc tmpH,dlyHi
    sts OCR1AH,tmpH ; start the first OC1A operation to start the high tone
    sts OCR1AL,tmpL ;   "
    ldi tmpH,0x02   ; enable OC1A interrupt locally
    sts TIMSK1,tmpH ;   "
    sts TIFR1,tmpH  ; clear OCF1A flag
    sei         ; enable interrupt globally
again:  ldi R16,5       ; wait for 0.5 s
    call    delayby100ms    ;   "
    ldi dlyHi,high(loCnt)   ; change delay count to that for 440-Hz
    ldi dlyLo,low(loCnt)    ;   "
    ldi R16,5       ; wait for 0.5 s
    call    delayby100ms    ;   "
    ldi dlyHi,high(hiCnt)   ; change delay count to that for 880-Hz
    ldi dlyLo,low(hiCnt);   "
    rjmp    again       ; jump to switch tone
; ------------------------------------------------------------------------------------------------------------↙
    --------
; The OC1AISR interrupt routine restart a new compare operation to OC1A using
; dlyHi:dlyLo as delay count.
; ------------------------------------------------------------------------------------------------------------↙
    --------
oc1AISR:    lds tmpL,OCR1AL
    lds tmpH,OCR1AH
    add tmpL,dlyLo
    adc tmpH,dlyHi  ;   "
    sts OCR1AH,tmpH ; start the next compare operation for
    sts OCR1AL,tmpL ; channel OC1A
    reti
; ------------------------------------------------------------------------------------------------------------↙
    ---------------
; The following subroutine uses Timer 3 to create a time delay that is a multiple of
```

```
; 100 ms. The multiple is passed in R16.
; ------------------------------------------------------------------------------------------------------------
    ---------------
    .def    tmp1 = r19
delayby100ms:
    ldi tmp1,0  ; configure Timer 3 to normal mode
    sts TCCR3A,tmp1 ; with clock source set to
    ldi tmp1,0x03   ; clk_IO / 64
    sts TCCR3B,tmp1 ;   "
wp100:  ldi tmp1,high(40536)    ; Let Timer1 count up from 40536 (2**16 - 25000) so that it
    sts TCNT3H,tmp1 ; overflows in 25000 clock cycles
    ldi tmp1,low(40536) ;   "
    sts TCNT3L,tmp1 ;   "
    ldi tmp1,1<<TOV3    ; clear TOV1 flag
    sts TIFR3,tmp1  ;   "
wt100:  lds tmp1,TIFR3  ; wait until TOV3 flag is set to 1
    sbrs    tmp1,TOV3   ;   "
    rjmp    wt100   ;   "
    dec r16
    brne    wp100
    ret
```