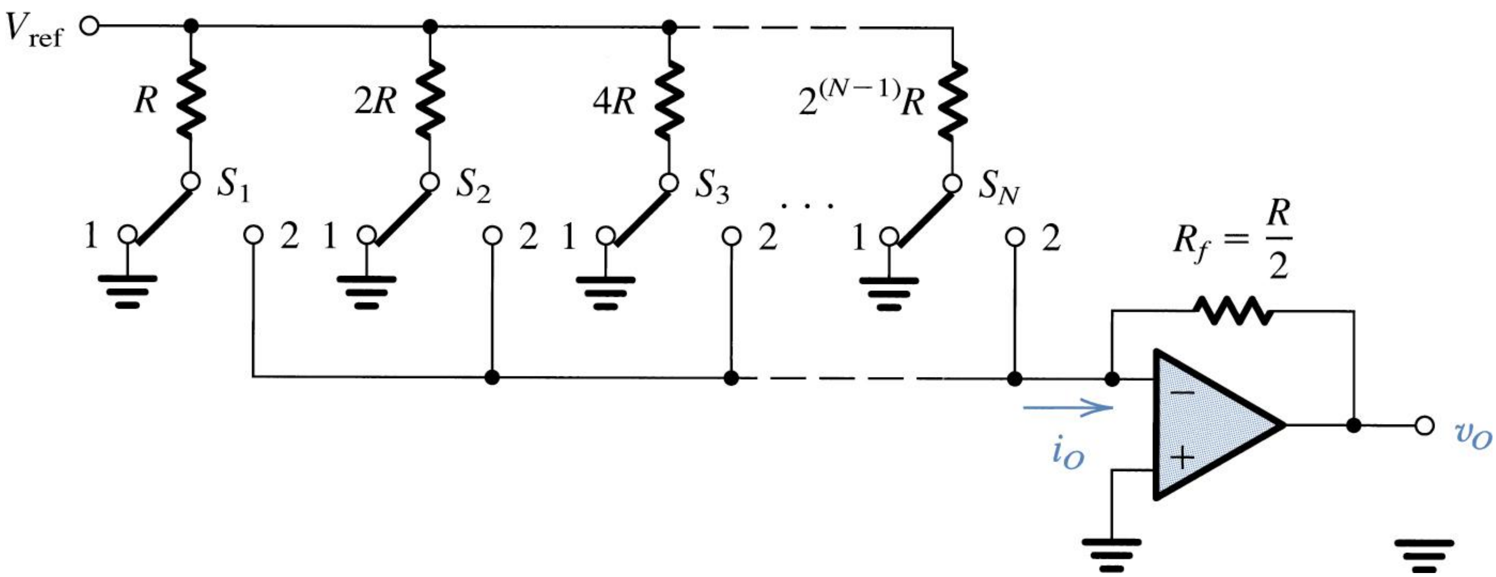
1) Basic circuit using binary-weighted resistor.
N binary-weighted resistors R, 2R, 2^2R,…2^{N-1}R



An N-bit D/A converter using a binary-weighted resistive ladder network.

N-bit digital input D: $b_1b_2b_3\ldots b_N$

Rewritten in decimal $D=\frac{b_1}{2^1}+\frac{b_2}{2^2}+\frac{b_3}{2^3}...+\frac{b_N}{2^N}$

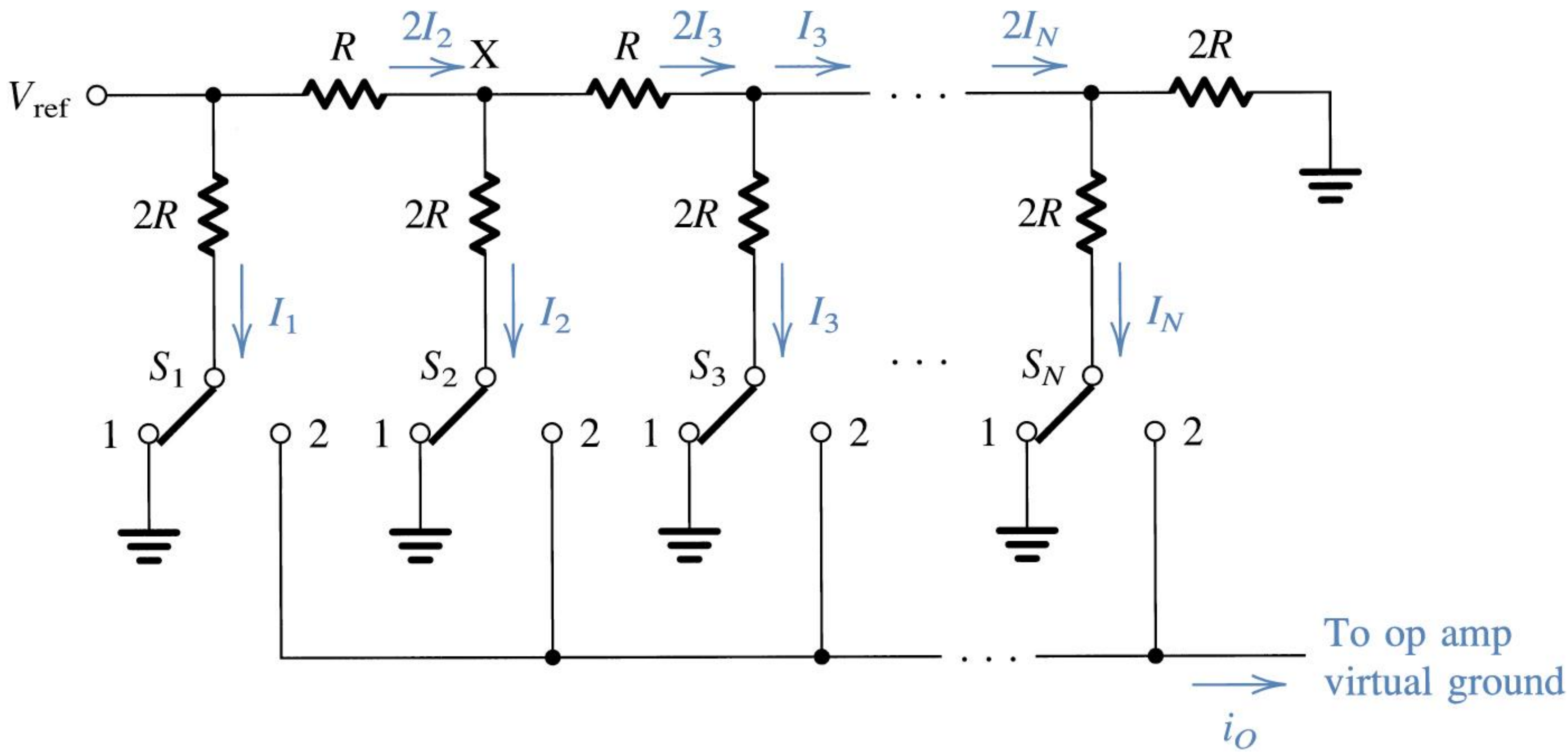
Where bi is the switch Si, bi=0, when switch is connecting to 1
bi=1, when switch is connecting to 2

$$i_o=\frac{V_{ref}}{R}b_1+\frac{V_{ref}}{2R}b_2+\frac{V_{ref}}{2^2R}b_3...+\frac{V_{ref}}{2^{N-1}R}b_N$$
$$=\frac{V_{ref}}{2R}(\frac{b_1}{2^1}+\frac{b_2}{2^2}+\frac{b_3}{2^3}...+\frac{b_N}{2^N})$$
$$=\frac{V_{ref}}{2R}D$$

$$Vo=-i_oR_f=-\frac{V_{ref}}{2R}D*R/2=V_{ref}D$$

Remarks: N increase, spread between R and 2^{N-1}R increases
Difficult to maintain accuracy in resistor value

2) Improved R-2R ladders

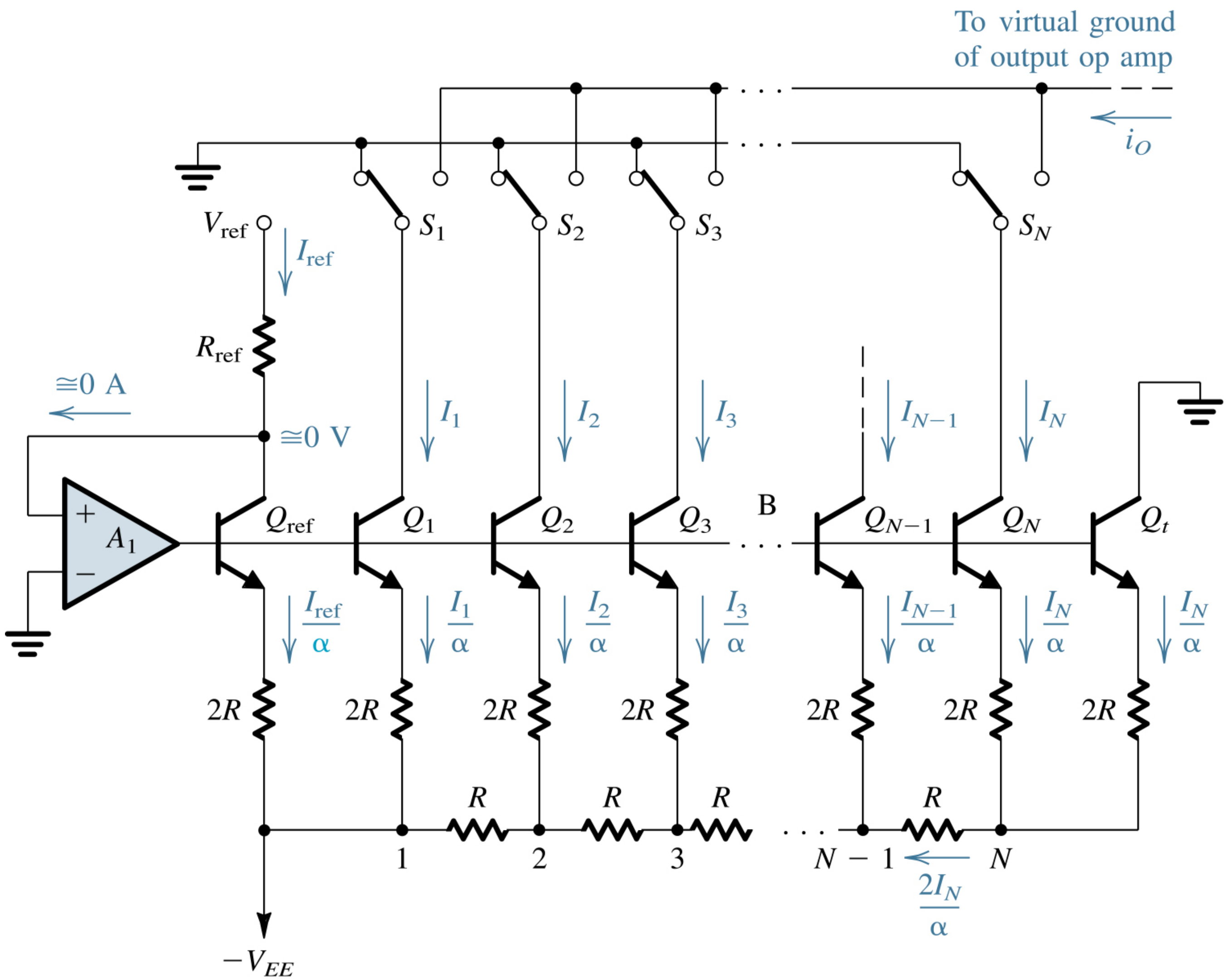


Basic circuit configurations of a DAC utilizing an *R*-2*R* ladder network.

$I_1 = 2I_2 = 4I_3 = ... = 2^{n-1} I_N$

$$i_o = \frac{V_{ref}}{R} D$$

3) A practical implementation of R-2R ladders



A practical circuit implementation of a DAC utilizing an *R*-2*R* ladder network.